REMARKS/ARGUMENTS

Reconsideration of the present application, as amended, is respectfully requested.

The September 27, 2005 Office Action and the Examiner's comments have been carefully considered. In response, claims are amended and remarks are set forth below in a sincere effort to place the present application in form for allowance. The amendments are supported by the application as originally filed. Therefore, no new matter is added.

PRIOR ART REJECTIONS

In the Office Action claims 1, 2, 4 and 5 are rejected under 35 USC 103(a) as being unpatentable over USP 6,493,019 (Hirasawa) in view of USP 6,259,467 (Hanna). Claims 3 and 6 are rejected under 35 USC 103(a) as being unpatentable over USP 6,219,085 (Hanna) in view of Hirasawa.

In response, claims 1 and 3 are amended to more clearly define the present claimed invention over the cited references.

Amended claim 1 is directed to a circuit for generating dot clock pulses utilized by an image-forming apparatus having an image-writing section, which includes:

> a digital-delay dot clock adjusting section to generate first dot clock pulses having a predetermined number of pulses within a predetermined time interval at a constant

exposing range of the image-writing section for making a correction against a deviation expanded or contracted, wherein each period of the first dot pulses is slightly increased or reduced by changing a successive selection for a plurality of delayed clock pulses, which are generated successively in slightly different delay times by delaying clock-pulses, output from a reference oscillator, in slightly different delay times; and

a jitter suppressing section to suppress a jitter component included in the first dot clock pulses, wherein the jitter suppressing section divides the first dot clock pulses to generate second dot clock pulses, and then, multiplies the second dot clock pulses to generate the dot clock pulses.

In the present claimed invention, the plurality of delayed clock pulses are successively generated by delaying reference clock-pulses and are successively selected so as to correct deviations to be generated in the created image (a digital-delay dot clock adjusting section). In order to overcome the problem that jitter is liable to occur in the above-mentioned configuration, a jitter suppressing section is provided for suppressing the jitter component included in the dot clock pulses. Accordingly, it is possible to obtain a high-quality image which is free from the influence of a jitter component in addition to the deviations.

The dot clock pulses, as shown in line (g) of Fig. 6, are obtained on the basis of the select signal, shown in line (e) of Fig. 6, generated by sequentially selecting each of the delayed dot clock pulses (DL50, DL49, DL48, DL47, DL46, DL45, DL44) from

the plurality of delayed dot clock pulses shown in Fig. 7. Then, the obtained dot clock pulses are input into the jitter suppressing section (420 shown in Fig. 9) to suppress the jitter component.

The invention as recited in amended claim 1 and as described above is not disclosed, taught, or suggested by Hirasawa or Hanna, or any of the other prior art of record.

USP 6,259,467 (Hanna) teaches as its object to obtain linearity of a picture element (PEL) row. For this purpose, a plurality of delayed clock pulses, shown in FIG. 4B, are generated by employing a MULTITAP DELAY 330 shown in Fig. 3A. Then, a specific one of the delayed clock pulses is selected for actual use (see claim 1 of Hanna). It is evident, however, that Hanna fails to disclose, teach or suggest a digital-delay dot clock adjusting section to generate first dot clock pulses having a predetermined number of pulses within a predetermined time interval at a constant exposing range of the image-writing section for making a correction against a deviation expanded or contracted, wherein the period of the first dot clock pulses is slightly increased or reduced by changing a successive selection for a plurality of delayed clock pulses, which are generated successively in slightly different delay times by delaying

clock-pulses, output from a reference oscillator, in slightly different delay times, as recited in amended claim 1.

USP 6,493,019 (Hirasawa) addresses the generation of jitter in the PLL circuit, and teaches a device for correcting such jitter. Hirasawa fails to disclose, teach or suggest a digital-delay dot clock adjusting section to generate first dot clock pulses having a predetermined number of pulses within a predetermined time interval at a constant exposing range of the image-writing section for making a correction against a deviation expanded or contracted, wherein the period of the first dot clock pulses is slightly increased or reduced by changing a successive selection for a plurality of delayed clock pulses, which are generated successively in slightly different delay times by delaying clock-pulses, output from a reference oscillator, in slightly different delay times, as recited in amended claim 1.

None of the other references of record close the gap between the present claimed invention as defined by claim 1 and Hanna taken either alone or in combination with Hirasawa. Therefore, claim 1 and claim 2 which is dependent on claim 1, are patentable over all of the references of record under 35 USC 102 as well as 35 USC 103.

Claim 3 includes the digital delay dot clock adjusting section recited in claim 1. Claim 3 is patentable over all of

the references of record for reasons, *inter alia*, set forth above in connection with claim 1.

Claims 4-6 are dependent on claim 3 and are patentable over the cited references in view of their dependence on claim 3 and because the references do not disclose, teach or suggest each of the limitations set forth in claims 4-6.

In view of all of the foregoing, claims 1-6 are patentable over the cited references under 35 USC 102 as well as 35 USC 103.

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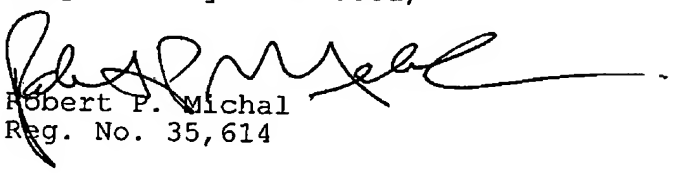
Entry of this Amendment, allowance of the claims and the passing of this application to issue are respectfully solicited.

If the Examiner disagrees with any of the foregoing, the Examiner is respectfully requested to point out where there is support for a contrary view.

If the Examiner has any comments, questions, objections or recommendations, the Examiner is invited to telephone the undersigned at the telephone number given below for prompt action.

Respectfully submitted,



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